What is claimed is:

1. A media access controller comprising:

a local bus for connecting blocks of the media access controller with each other;

a CPU connected with the local bus to drive the media access controller;

a register unit connected with the local bus to store information used for software control of the CPU with respect to internal units of the media access controller;

a host interface unit connected with the local bus to manage an interface between the media access controller and a host;

a physical layer interface unit connected with the local bus to manage an interface between the media access controller and a physical layer;

a power-save master for generating a signal for requesting an occupation/occupation expiration of the local bus in response to a signal inputted via the local bus and a value of the register;

a bus arbiter for generating a signal controlling a use of the local bus in response to the signal generated from the power-save master;

a power control unit for generating signals determining whether to supply clocks and power to the respective blocks of the media access controller, in response to the control signal of the bus arbiter, the register values inputted via the local bus, and a power-save mode exiting signal provided from other blocks of the media access controller;

a phase-locked loop for generating clocks in response to the signal determining whether to supply the power, the signal being generated from the power control unit;

a clock generator receiving the phase-locked clock from the phase-locked loop to generate clocks required to the media access controller, and supplying or disabling the clocks

generated according to the signal determining whether to supply the clock, the signal being generated from the power control unit; and

a wake-up timer for applying a power-save mode exiting signal to the power control unit in response to the signals inputted from the local bus and the clock generator.

2. The media access controller of claim 1, wherein a direct connection method is employed when supplying the power and clocks to respective processors of the media access controller according to the power-save mode exiting signal.

3. The media access controller of claim 1, wherein the register unit includes a clock disable register and a locktime register.

4. The media access controller of claim 3, wherein the locktime register stores a time required until an output of the phase-locked loop is settled.

5. The media access controller of claim 1, wherein the power control unit generates a plurality of state control signals PLL_PWDN, PLL_STA and CLK_EN for controlling the power and clocks of the media access controller, in response to a first control signal MST from the bus arbiter, a second control signal WKUP from the wake-up timer, a first input value VLOC from the locktime register, and a second input value VSTB from the clock disable register.

6. The media access controller of claim 5, wherein the power-save master generates one signal for requesting the occupation/occupation expiration of the bus, in

response to the second input value VSTB from the clock disable register and the signal PLL_STA from the power control unit.

7. The media access controller of claim 6, wherein the power-save master is implemented with one register.

8. The media access controller of claim 1, wherein the power-save master generates one signal for requesting the occupation/occupation expiration of the bus, in response to the second input value VSTB from the clock disable register and the signal PLL_STA from the power control unit.

9. The media access controller of claim 1, wherein the clock generator supplies or disables the clocks to the respective blocks of the media access controller in response to any one of the state control signals generated from the power control unit.

10. The media access controller of claim 1, wherein the wake-up timer includes a wake-up time register for storing a time DTIM and a wake-up count register for counting the time DTIM.

11. The media access controller of claim 9, wherein the wake-up timer copies the time DTIM of the wake-up time register into the wake-up count register in response to a control signal MST from the bus arbiter in the power-save mode, and counts a value of the wake-up time register in synchronization with a low-speed clock divided from the clock generator.

12. A method of changing a media access controller to a power-save mode, comprising the steps of:

(a) initializing the media access controller by supplying power thereto;

(b) operating normally the media access controller in an active mode;

(c) selecting the power-save mode of the media access controller;

(d) setting a power control register of a physical layer interface unit provided within the media access controller;

(e) setting a wake-up time value to a wake-up time register of the media access controller;

(f) setting a stop bit to a clock disable register of the media access controller;

(g) transmitting a bus occupation request signal from a power-save master of the media access controller to a bus arbiter;

(h) checking whether or not there is a bus master which currently uses a bus of the media access controller;

(i) disabling clocks supplied to the media access controller; and

(j) powering down a phase-locked loop of the media access controller.

13. The method of claim 12, wherein a locktime value is set to a locktime register of the media access controller at the step (a).

14. The method of claim 13, wherein the locktime value is a power stabilization time of the phase-locked loop of the media access controller.

15. The method of claim 12, wherein clocks supplied to external blocks connected with the media access controller are disabled by the value of the power control register set at the step (d).

16. The method of claim 12, wherein the value of the wake-up time register set at the step (e) is a power-save maintaining time of the media access controller.

17. A method of changing a media access controller from a power-save mode to an active mode, comprising the steps of:

(a) decreasing a value of a wake-up count register of the media access controller one bit by one bit until the value of the wake-up count register becomes one;

(b) supplying a power to a phase-locked loop of the media access controller when the value of the wake-up count register becomes one;

(c) decreasing a value of a locktime register of the media access controller one bit by one bit until the value of the locktime register becomes zero;

(d) providing clocks to the media access controller;

(e) expiring a bus occupation of a power-save master of the media access controller; and

(e) clearing a stop bit stored in a clock disable register of the media access controller.

18. The method of claim 17, wherein the processes of changing the media access controller from the power-save mode to the active mode are achieved only through hardware.